ABSTRACT OF THE DISCLOSURE

A method is disclosed for synthesizing a clock tree for a partitioned integrated circuit (IC) layout comprising a plurality of base level partitions and a top level partition each occupying a separate area of a semiconductor substrate, The base level partitions include syncs to be clocked by edges of a clock signal applied to an entry node within the area occupied by the top level partition. In accordance with the method, a plurality of independently balanced subtrees are separately synthesized. Each subtree resides within the area occupied by a separate base level partition and includes a start point at a perimeter of the area occupied by that base level partition and a network of buffers and signal paths for conveying a clock signal edge from the start point to each sync included within that area. Thereafter a top level portion of the clock tree is synthesized. The top level portion of the subtree resides within the substrate area containing the top level partition and conveys the clock signal from the entry point to the start point of each synthesized subtree.